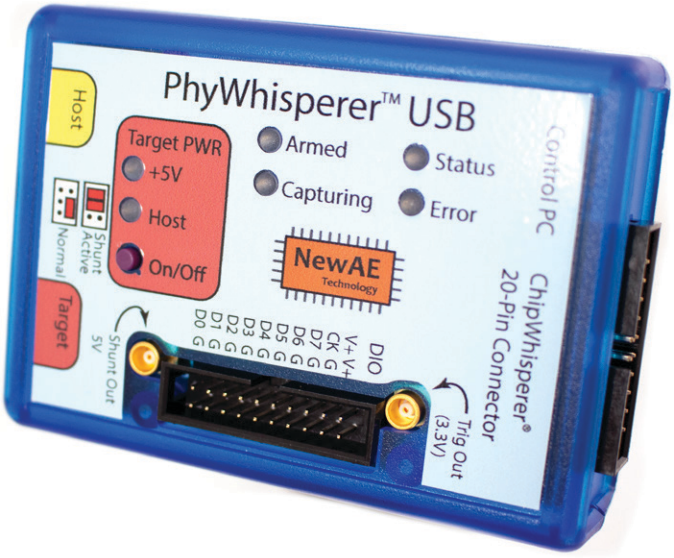
NewAE Technology Inc.
newae.com

ChipWhisperer® Embedded Security Analysis Tools
Triggering Tools

CW610: PhyWhisperer® USB

Product Datasheet



The PhyWhisperer® toolchain is designed for exploring physical layer protocols. The PhyWhisperer-USB is a fully open source (hardware, firmware, FPGA code, software) tool that can sniff USB 2.0 LS/FS/HS traffic.

It is primarily designed to work with the ChipWhisperer® and ChipSHOUTER® tools from NewAE Technology Inc., by serving as a unit to trigger on USB protocols with high accuracy.

The device allows offsetting the output trigger pulse from the actual event, as would be required during fault injection testing.

A built-in shunt allows monitoring power consumption on an external oscilloscope or ChipWhisperer, in order to perform power analysis over the USB power line.

Product Highlights

USB PHY front-end allows monitoring of USB 2.0 LS/FS/HS traffic.

Python control interface (API) for viewing of raw USB data, or piping data into analysis tools such as ViewSB.

Trigger on USB packets for fault injection or side-channel analysis triggering.

Programmable trigger offset delay & width to directly drive fault injection equipment such as ChipSHOUTER.

Convenient front-panel button allows power-cycling of target device (also accessible by API).

20-pin connector interfaces directly to ChipWhisperer for providing clock & trigger synchronization.

Expansion connector allows investigating other protocols (requires FPGA programming), with planned support for Arm Trace (ETM) and Ethernet protocols.

Translucent blue enclosure gentle reminder of the lure of the sea.

Ordering Summary

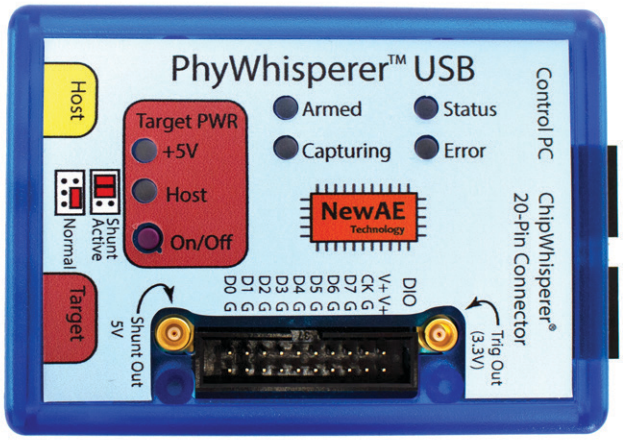
NAE-PHYWHISPERERUSB	PhyWhisperer-USB main unit with (2) micro-USB cables, (1) MCX to SMA cable, and (1) MCX to BNC cable.

Product Links

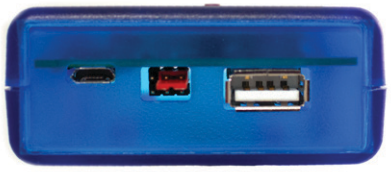
Full Documentation	http://www.phywhisperer.com

Specifications & Photos

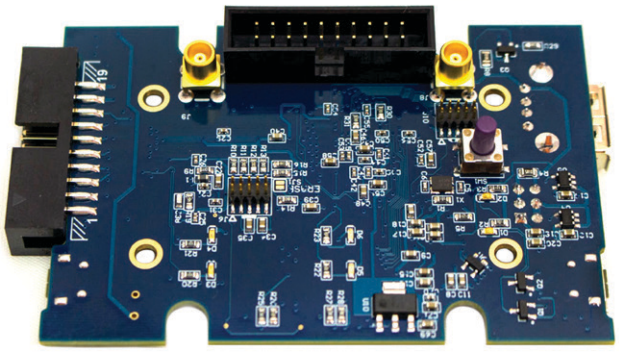
Feature/Specification	Notes/Range
USB Modes supported	USB 2.0 Low/Full/High-Speed.
FPGA	Xilinx Spartan 7S15.
FPGA Configuration	FPGA reconfigured through Python interface (no hardware needed).
Control PC connection	Micro-USB 2.0 HS.
Host USB connection	Micro-USB.
Target USB connection	Female A Connector.
Target power supply	Host USB or Control PC (software selectable with on/off).
Spare digital I/O	8 data pins, 1 clock pin routed to FPGA via 0.1"x0.1" male header.
Trigger pattern	1 - 64 bytes with mask.
Trigger delay	0 - 1048576 cycles of 240 MHz internal clock (derived from USB clock).
USB sniffer FIFO	8192 bytes.
Size	94 x 66 x 27 mm (0.10 x 0.072 x 0.030 yards)
Weight	90 g (0.000099 US Tons, 0.000089 British Tons, 0.000090 Metric Tons)
Colour	Translucent Blue.
Smell	Plastic.
Cursed	No.



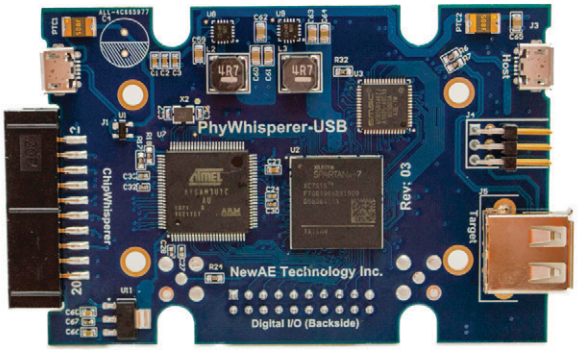
Front Panel Connections



Target connections

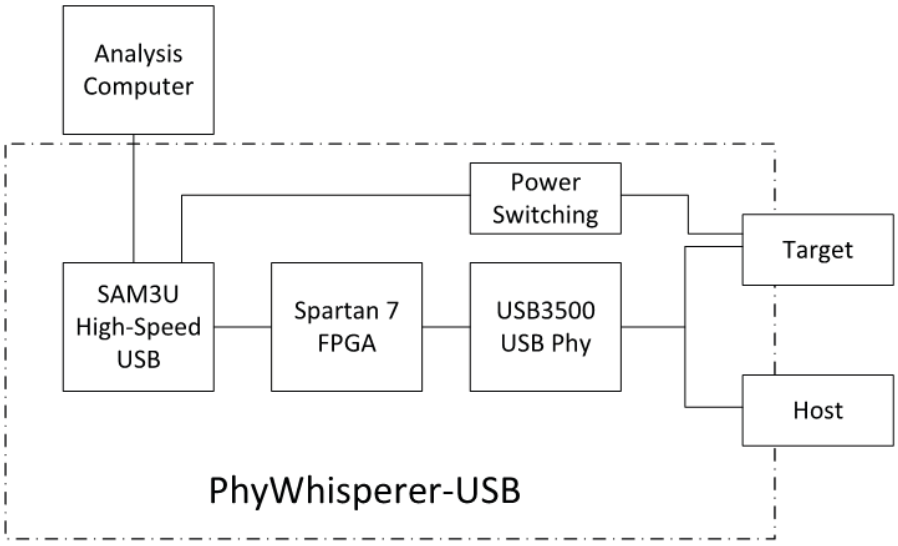


PCB Board (Facing Front)



PCB Board (Facing Into Case)

Design Overview



A USB3500 front-end provides a simple parallel interface to the Spartan 7S15 FPGA. This allows the device to monitor the USB traffic in real-time, along with triggering on bytes in the USB datastream. This device uses a ATSAM3U1C microcontroller as the high-speed USB interface to the host PC. The use of the AT-SAM3U1C provides flexibility to run code on the microcontroller for other tasks. Because the system is fully open-source, you can use this for your own development.

The USB front-end has a number of jumpers to allow routing of power in various ways. By default you can use it as a simple sniffer, but by adjusting some jumpers, you can insert a 5-ohm shunt resistor into the USB power line. This shunt resistor allows 'simple power analysis' to be performed on a device. The output of the shunt is routed to an MCX connector on the front-panel.

See GITHub links for detailed design including PCB design sources, FPGA designs, microcontroller firmware, and software for PC interface.

Disclaimers